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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,471	09/15/2003	Omer H. Dokumaci	YOR920020233US1	2890

7590 05/12/2005

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EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,471	DOKUMACI ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/15/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-18, drawn to a method, classified in class 438, subclass 706.

II. Claims 19-20, drawn to a transistor, classified in class 257, subclass 66.

2. The inventions are distinct, each from the other because of the following reasons: Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the method as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different method (MPEP § 806.05(f)). In the instant case, the product can be manufactured with wet etching rather than dry etching or high-temperature diffusion rather than ion implantation. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

3. During a telephone conversation with Eric W. Petraske on April 26, 2005 a provisional election was made without traverse to prosecute Invention I, claims 1-18. Affirmation of this election must be made by applicant in replying to this Office action. Claims 19-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Priority

5. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1-5 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yagishita et al. (U.S. Patent No. 6,465,823), in view of Liu et al. (U.S. Patent No. 5,712,173).

9. As to claim 1, Yagishita discloses a method of forming a double-gate transistor comprising the steps of: providing a semiconductor wafer having a substrate and a device layer (1003), a back gate dielectric layer (1002) adjacent to and below said Device layer, a back gate electrode (1001) between said back gate dielectric layer and said substrate (column 15, lines 9-14; Figure 8A), a front gate dielectric (1005) on said Device layer and a front gate electrode layer (1101) on said front gate dielectric layer; depositing at least one transfer layer (1102) on said front gate electrode layer (1101); patterning said at least one transfer layer with a gate pattern and forming a first gate (1003b) in said front gate electrode layer using said transfer layer as a mask (column 15, lines 15-23); forming at least one vertical spacer layer (1010/1103) adjacent to opposite sides of said front gate (column 15, lines 24-30, lines 49-53; Figures 8C-8E); etching said Device layer using said at least one spacer layer (1010) as a mask to form a transistor body disposed on said back gate dielectric layer (column 15, lines 32-35); and forming source and drain electrodes (1012) on opposite sides of said transistor body (column 16, lines 49-52; Figure 8P).

10. Yagishita does not expressly disclose oxidizing said back gate electrode (1002) such that oxide is formed below said transistor body and on either side of a central

portion of said back gate electrode, thereby forming said back gate self-aligned with said front gate. However, Liu discloses a method of forming buried oxide layers by implanting oxygen into the exposed portions of the substrate, using the gate mask and gate electrode as a mask (column 4, lines 48-52). Liu teaches that buried oxide layers are important in minimizing junction capacitance (column 4, lines 39-40). Implantation is followed by an annealing step, such that the implanted oxygen reacts with the substrate (column 4, lines 52-55). Moreover, Liu's method produces a buried oxide that is aligned with the electrodes and does not require additional masking steps (column 4, lines 48-52). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to oxidize said back gate electrode such that oxide is formed below said transistor body and on either side of a central portion of said back gate electrode, thereby forming said back gate self-aligned with said front gate. One who is skilled in the art would be motivated to form buried oxide structures that are self-aligned and does not require additional masking steps.

11. As to claim 2, Yagishita disclose that step of forming at least one vertical spacer comprises forming a first vertical spacer (1010) in proximity to said front gate and having a bottom surface above said transistor body (column 15, lines 24-28; Figure 8C); thereafter performing said step of etching said Device layer to form said transistor body (column 15, lines 32-35); and forming a second spacer (1103) in proximity to a vertical edge of said transistor body (column 15, lines 49-53; Figure 8E).

12. As to claim 3, Yagishita does not expressly disclose that oxidizing said back gate electrode is performed with at least one vertical spacer (1010) disposed in proximity to a

vertical edge of said transistor body, thereby defining a lateral extent of oxidation by the thickness of said vertical spacer, said oxidation extending underneath said vertical spacer and said transistor body and into said back gate electrode. Liu discloses a method of forming buried oxide layers by implanting oxygen into the exposed portions of the substrate, using the gate mask and gate electrode as a mask (column 4, lines 48-52). Liu teaches that buried oxide layers are important in minimizing junction capacitance (column 4, lines 39-40). Implantation is followed by an annealing step, such that the implanted oxygen reacts with the substrate (column 4, lines 52-55). During anneal, Liu teaches that the oxide layer may extend laterally under the gate electrode (column 4, lines 59-64). Thus, oxidation will inherently extend underneath said vertical spacer and said transistor body. Moreover, Liu's method produces a buried oxide that is aligned with the electrodes and does not require additional masking steps (column 4, lines 48-52). Yagishita discloses that vertical spacer (1010) is used as an etch mask for the etching of device layer (1003) (column 15, lines 32-35). Thus, vertical spacer (1010) can be utilized a second time as a mask for the oxygen ion implantation step. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: oxidizing said back gate electrode with at least one vertical spacer disposed in proximity to a vertical edge of said transistor body, thereby defining a lateral extent of oxidation by the thickness of said vertical spacer, said oxidation extending underneath said vertical spacer and said transistor body and into said back gate electrode. One who is skilled in the art would be

motivated to form buried oxide structures that are self-aligned and does not require additional masking steps.

13. As to claim 4, Yagishita does not expressly disclose that oxidizing said back gate electrode is performed with said second vertical spacer (1103) disposed in proximity to a vertical edge of said transistor body, thereby defining a lateral extent of oxidation by the thickness of said second vertical spacer, said oxidation extending underneath said vertical spacer and said transistor body and into said back gate electrode. Liu discloses a method of forming buried oxide layers by implanting oxygen into the exposed portions of the substrate, using the gate mask and gate electrode as a mask (column 4, lines 48-52). Liu teaches that buried oxide layers are important in minimizing junction capacitance (column 4, lines 39-40). Implantation is followed by an annealing step, such that the implanted oxygen reacts with the substrate (column 4, lines 52-55). During anneal, Liu teaches that the oxide layer may extend laterally under the gate electrode (column 4, lines 59-64). Thus, oxidation will inherently extend underneath said vertical spacer and said transistor body. Moreover, Liu's method produces a buried oxide that is aligned with the electrodes and does not require additional masking steps (column 4, lines 48-52). Yagishita discloses that vertical spacer (1103) is used as a spacer for forming electrode (1012) (column 16, lines 34-36, lines 49-52). Thus, vertical spacer (1103) can be utilized a second time as a mask for the oxygen ion implantation step. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of: oxidizing said back gate electrode with said second vertical spacer disposed in proximity to a vertical edge of

said transistor body, thereby defining a lateral extent of oxidation by the thickness of said second vertical spacer, said oxidation extending underneath said vertical spacer and said transistor body and into said back gate electrode. One who is skilled in the art would be motivated to form buried oxide structures that are self-aligned and does not require additional masking steps.

14. As to claim 5, Yagishita discloses that a step of depositing a layer of interlevel dielectric (1013) about said transistor up to at least the top of said front gate (column 15, lines 54-57; Figure 8F), stripping said second vertical spacer (1103), thereby forming an aperture (1107) over the source and drain of said transistor (column 16, lines 34-36; Figure 8O), and depositing a conductive material in said aperture, thereby forming a raised S/D structure (column 16, lines 49-52; Figure 8P).

15. As to claims 9-11, Liu does not expressly disclose performing an angled implantation into said back gate electrode of an ion species that promotes oxidation before said step of oxidation, thereby increasing the rate of oxidation in the implanted area. Liu discloses a method of forming buried oxide layers by implanting oxygen into the exposed portions of the substrate, using the gate mask and gate electrode as a mask (column 4, lines 48-52). Liu teaches that buried oxide layers are important in minimizing junction capacitance (column 4, lines 39-40). Implantation is followed by an annealing step, such that the implanted oxygen reacts with the substrate (column 4, lines 52-55). During anneal, Liu teaches that the oxide layer may extend laterally under the gate electrode (column 4, lines 59-64). At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to

perform an angled implantation because applicant has not disclosed that performing an angled implantation provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicants' invention to perform equally well with annealing the implanted region such that it extends laterally because both annealing and performing an angled implantation perform the same function.

16. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yagishita, in view of Liu, in further view of Doyle et al. (U.S. Patent No. 5,891,798).

17. As to claim 14, Liu does not expressly disclose performing a vertical implantation into said back gate electrode of an ion species that retards oxidation before said step of oxidation, thereby decreasing the rate of oxidation in the vertical direction. However, Doyle teaches a method of preventing oxygen diffusion into a substrate (105) (column 1, lines 33-40) by nitriding the substrate (column 1, lines 45-48). Moreover, Doyle teaches that nitriding can be accomplished by implanting nitrogen into the substrate (column 2, lines 48-65) to prevent the oxidation of the silicon surface (column 3, lines 7-9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform a vertical implantation into said back gate electrode of an ion species that retards oxidation before said step of oxidation, thereby decreasing the rate of oxidation in the vertical direction. One who is skilled in the art would be motivated to implant nitrogen into the substrate, because it is a successful technique for controlling diffusion of oxygen in silicon.

18. Claims 6-8 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yagishita, in view of Liu, in further view of Wu (U.S. Patent No. 6,117,711).

19. As to claim 6, Liu does not expressly disclose that the step of oxidizing is conducted at a temperature of at least 1000°C for a time sufficient to reduce stress in said transistor body. Liu teaches that implantation is followed by an annealing step, such that the implanted oxygen reacts with the substrate (column 4, lines 52-55). However, Wu discloses that following oxygen ion implantation, the buried region is amorphous and is converted to oxide by heating from 1050°C to 1350°C (column 3, lines 30-38). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of oxidizing at a temperature of at least 1000°C for a time sufficient to reduce stress in said transistor body. One who is skilled in the art would be motivated to anneal the implanted region at a temperature range that has been established for convert the amorphous region to oxide.

20. As to claims 7-8, Liu does not expressly disclose that the step of oxidizing is conducted at a temperature of at least 1000°C for at least twenty minutes. Liu teaches that implantation is followed by an annealing step, such that the implanted oxygen reacts with the substrate (column 4, lines 52-55). However, Wu discloses that following oxygen ion implantation, the buried region is amorphous and is converted to oxide by heating from 1050°C to 1350°C (column 3, lines 30-38). Furthermore, thickness of the oxide layer is controlled by time and temperature (column 3, lines 37-38). Moreover, Wu teaches, by disclosing that annealing time may be varied, that changing annealing time appears to reflect a result-effective variable which can be optimized. *See* MPEP §

2144.05 II. Annealing time can be varied according, depending on the desired thickness of the buried oxide layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to oxidize at a temperature of at least 1000°C for at least twenty minutes. One who is skilled in the art would be motivated to optimize the thickness of the buried oxide layer through routine experimentation of annealing time. *See* MPEP § 2144.05 II.

21. As to claims 12-13, Liu does not expressly disclose performing an angled implantation into said back gate electrode of an ion species that promotes oxidation before said step of oxidation, thereby increasing the rate of oxidation in the implanted area. Liu discloses a method of forming buried oxide layers by implanting oxygen into the exposed portions of the substrate, using the gate mask and gate electrode as a mask (column 4, lines 48-52). Liu teaches that buried oxide layers are important in minimizing junction capacitance (column 4, lines 39-40). Implantation is followed by an annealing step, such that the implanted oxygen reacts with the substrate (column 4, lines 52-55). During anneal, Liu teaches that the oxide layer may extend laterally under the gate electrode (column 4, lines 59-64). At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to perform an angled implantation because applicant has not disclosed that performing an angled implantation provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicants' invention to perform equally well with annealing the implanted region such

that it extends laterally because both annealing and performing an angled implantation perform the same function.

22. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yagishita, in view of Liu, in further view of Wu, in further view of Doyle.

23. As to claims 15-17, Liu does not expressly disclose performing a vertical implantation into said back gate electrode of an ion species that retards oxidation before said step of oxidation, thereby decreasing the rate of oxidation in the vertical direction. However, Doyle teaches a method of preventing oxygen diffusion into a substrate (105) (column 1, lines 33-40) by nitriding the substrate (column 1, lines 45-48). Moreover, Doyle teaches that nitriding can be accomplished by implanting nitrogen into the substrate (column 2, lines 48-65) to prevent the oxidation of the silicon surface (column 3, lines 7-9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform a vertical implantation into said back gate electrode of an ion species that retards oxidation before said step of oxidation, thereby decreasing the rate of oxidation in the vertical direction. One who is skilled in the art would be motivated to implant nitrogen into the substrate, because it is a successful technique for controlling diffusion of oxygen in silicon.

24. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yagishita, in view of Liu, in further view of Wolf, *Silicon Processing for the VLSI Era*, Vol. 4, Lattice Press (2002).

25. As to claim 18, Yagishita discloses a method of forming a double-gate transistor comprising the steps of: forming a back gate electrode (1001); forming a back gate

dielectric layer (1002); forming a device layer (1003) (column 14, lines 1-4); forming a front gate dielectric (1005) on said device layer (1003); forming a front gate electrode layer (1101) on said front gate dielectric layer (1005) (column 15, lines 9-14; Figure 8A); depositing at least one transfer layer (1102) on said front gate dielectric (1101); patterning said at least one transfer layer with a gate pattern and forming a first gate (1003b) in said front gate electrode layer (column 15, lines 15-23); forming at least one vertical spacer layer (1010/1103) adjacent to opposite sides of said first gate (column 15, lines 24-30, lines 49-53; Figures 8C-8E); etching said device layer using said at least one spacer layer (1010) as a mask to form a transistor body disposed on said back gate dielectric layer (column 15, lines 32-35); and forming source and drain electrodes (1012) on opposite sides of said transistor body (column 16, lines 49-52; Figure 8P).

26. Yagishita does not expressly disclose forming the structure with a wafer bonding technique, including the steps of: providing an SOI wafer having a first substrate, a BOX layer and a device layer; forming a back gate dielectric layer on said device layer; forming a back gate electrode on said back gate dielectric layer; bonding a second wafer having a second substrate to said back gate electrode of said SOI wafer; removing said first substrate; and removing said BOX layer. However, Wolf teaches that the wafer bonding is a popular technology for producing silicon on insulator wafers (page 537). Moreover, the technique involves at least one thermally oxidized silicon wafer and one bare wafer, which are bonded by applying pressure at room temperature and annealing (pages 538-39). The next step is to remove most of the silicon from one

wafers and constructing the semiconductor device on the remaining thinned silicon wafer (page 540). At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to perform wafer bonding to fabricate the structure because applicant has not disclosed that wafer bonding provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicants' invention to perform equally well with conventional deposition of layers because both conventional deposition of layers and wafer bonding are techniques that can produce an equivalent structure.

27. Yagishita does not expressly disclose oxidizing said back gate electrode (1002) such that oxide is formed below said transistor body and on either side of a central portion of said back gate electrode, thereby forming said back gate self-aligned with said first gate. However, Liu discloses a method of forming buried oxide layers by implanting oxygen into the exposed portions of the substrate, using the gate mask and gate electrode as a mask (column 4, lines 48-52). Liu teaches that buried oxide layers are important in minimizing junction capacitance (column 4, lines 39-40). Implantation is followed by an annealing step, such that the implanted oxygen reacts with the substrate (column 4, lines 52-55). Moreover, Liu's method produces a buried oxide that is aligned with the electrodes and does not require additional masking steps (column 4, lines 48-52). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to oxidizing said back gate electrode such that oxide is formed below said transistor body and on either side of a central portion of said back

gate electrode, thereby forming said back gate self-aligned with said front gate. One who is skilled in the art would be motivated to form buried oxide structures that are self-aligned and does not require additional masking steps.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC EBC
May 9, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER